Amendments to the Claims

1. (Currently Amended): A method of forming memory circuitry comprising:

providing a semiconductor substrate comprising a pair of word lines having a bit node received therebetween, insulative sidewall spacers being received over opposing sidewalls of the word lines facing the bit node;

depositing insulative material over the pair of word lines, the bit node and the insulative sidewall spacers;

forming a bit node contact opening within the insulative material over the bit node;

forming sacrificial plugging material within the bit node contact opening between the pair of word lines;

~~removing sacrificial plugging material~~ from the bit node contact opening, removing sacrificial plugging material which is received between and at some common elevation with conductive portions of the pair of word lines, and replacing it with conductive material in the bit node contact opening that is in electrical connection with the bit node; and

after the replacing, forming the conductive material into a bit line.

2. (Original): The method of claim 1 wherein the sacrificial plugging material comprises insulative material.

3. (Original): The method of claim 1 wherein the sacrificial plugging material comprises conductive material.

4. (Original): The method of claim 1 wherein the sacrificial plugging material comprises conductively doped semiconductive material.

5. (Original): The method of claim 1 wherein the sacrificial plugging material comprises semiconductive material.

6. (Original): The method of claim 1 wherein the sacrificial plugging material comprises insulative material and semiconductive material.

7. (Original): The method of claim 6 wherein the insulative material comprises silicon dioxide and the semiconductive material comprises polysilicon.

8. (Original): The method of claim 1 wherein prior to the removing, depositing an insulating layer and etching a removal opening through it to the sacrificial plugging material, the removing comprising etching the sacrificial plugging material from the bit node contact opening through the removal opening.

9. (Original): The method of claim 1 wherein the forming of the conductive material into a bit line comprises lithography and etch.

10. (Original): The method of claim 1 comprising forming a capacitor of a memory cell of the memory circuitry after forming the bit line.

11. (Original): The method of claim 10 comprising forming an elevationally outermost electrode of the capacitor to be received everywhere elevationally outer of the bit line.

12. (Original): The method of claim 1 comprising prior to the removing, polishing the insulative material and the sacrificial plugging material.

13. (Currently Amended): A method of forming memory circuitry comprising buried bit line memory cells, comprising:

providing a semiconductor substrate comprising a first pair of word lines having a bit node received therebetween and a second pair of word lines having a capacitor node received therebetween;

commonly forming ~~a bit node~~ 1) a bit node contact opening within insulative material over the bit node and ~~a capacitor node~~ 2) a capacitor node contact opening within insulative material over the capacitor node;

commonly forming sacrificial plugging material within ~~the bit node~~ 1) the bit node contact opening and ~~within the capacitor node~~ 2) the capacitor node contact opening;

removing sacrificial plugging material from the bit node contact opening while leaving sacrificial plugging material within the capacitor node contact opening;

replacing the removed sacrificial plugging material from the bit node contact opening with conductive material that is in electrical connection with the bit node;

after the replacing, forming the conductive material into a bit line; and

after forming the bit line, removing sacrificial plugging material from the capacitor node contact opening.

14. (Original): The method of claim 13 wherein prior to removing sacrificial plugging material from the bit node contact opening, depositing an insulating layer and etching a removal opening through it to the sacrificial plugging material within the bit contact opening, the removing of sacrificial plugging material from the bit node contact opening comprising etching the sacrificial plugging material from the bit node contact opening through the removal opening.

15. (Original): The method of claim 13 comprising after removing the sacrificial plugging material from the capacitor node contact opening, forming a capacitor of a memory cell of the memory circuitry in electrical connection with the capacitor node.

16. (Original): The method of claim 13 wherein the sacrificial plugging material comprises insulative material.

17. (Original): The method of claim 13 wherein the sacrificial plugging material comprises conductive material.

18. (Original): The method of claim 17 wherein the sacrificial plugging material comprises conductively doped semiconductive material.

19. (Original): The method of claim 13 wherein the sacrificial plugging material comprises semiconductive material.

20. (Original): The method of claim 13 wherein the sacrificial plugging material comprises insulative material and semiconductive material.

21. (Original): The method of claim 20 wherein the insulative material comprises silicon dioxide and the semiconductive material comprises polysilicon.

22. (Original): The method of claim 13 comprising prior to the removing, polishing the insulative material and the sacrificial plugging material.

23. (Currently Amended): A method of forming memory circuitry comprising:

providing a semiconductor substrate having a memory array area and a peripheral circuitry area peripheral to the memory array area, the substrate comprising a first pair of word lines having a bit node received therebetween, the bit node being received within the memory array area;

commonly forming ~~a bit node contact~~ 1) a bit node contact opening within insulative material over the bit node, ~~a first peripheral contact~~ 2) a first peripheral contact opening within insulative material over a first node in the peripheral circuitry area, and ~~a second peripheral contact~~ 3) a second peripheral contact opening within insulative material over a second node in the peripheral circuitry area;

forming sacrificial plugging material within the bit node contact opening, the first peripheral contact opening and the second peripheral contact opening;

removing sacrificial plugging material from the bit node contact opening, the first peripheral contact opening and the second peripheral contact opening, and replacing it with conductive material that is in electrical connection with the bit node, the first node and the second node; and

after the replacing, forming the conductive material into a bit line in electrical connection with the bit node and into a local interconnect line in the peripheral circuitry area electrically interconnecting the first and second nodes.

24. (Original): The method of claim 23 wherein the forming sacrificial plugging material within the bit node contact opening, the first peripheral contact opening and the second peripheral contact opening comprises commonly forming sacrificial plugging material within the bit node contact opening, the first peripheral contact opening and the second peripheral contact opening.

25. (Original): The method of claim 23 wherein the forming of the conductive material into the bit line and into the local interconnect line comprises lithography and etch using at least some common lithographic and etching steps.

26. (Original): The method of claim 23 comprising forming a capacitor of a memory cell of the memory circuitry after forming the bit line and the interconnect line.

27. (Original): The method of claim 23 wherein prior to the removing, depositing an insulating layer and etching respective removal openings through it to the sacrificial plugging material within the bit node contact opening, the first peripheral contact opening and the second peripheral contact opening; the removing comprising etching the sacrificial plugging material from the bit node contact opening, the first peripheral contact opening and the second peripheral contact opening through the removal openings.

28. (Original): The method of claim 23 wherein the sacrificial plugging material comprises insulative material.

29. (Original): The method of claim 23 wherein the sacrificial plugging material comprises conductive material.

30. (Original): The method of claim 29 wherein the sacrificial plugging material comprises conductively doped semiconductive material.

31. (Original): The method of claim 23 wherein the sacrificial plugging material comprises semiconductive material.

32. (Original): The method of claim 23 wherein the sacrificial plugging material comprises insulative material and semiconductive material.

33. (Original): The method of claim 32 wherein the insulative material comprises silicon dioxide and the semiconductive material comprises polysilicon.

34. (Original): The method of claim 23 comprising prior to the removing, polishing the insulative material and the sacrificial plugging material.

35. (Currently Amended): A method of forming memory circuitry comprising buried bit line memory cells, comprising:

providing a semiconductor substrate having a memory array area and a peripheral circuitry area peripheral to the memory array area, the substrate comprising a first pair of word lines having a bit node received therebetween and a second pair of word lines having a capacitor node received therebetween, the bit node and the capacitor node being received within the memory array area;

commonly forming ~~a bit node contact~~ 1) a bit node contact opening within insulative material over the bit node, ~~a capacitor node contact~~ 2) a capacitor node contact opening within insulative material over the capacitor node, ~~a first peripheral contact~~ 3) a first peripheral contact opening within insulative material over a first node in the peripheral circuitry area, and ~~a second peripheral contact~~ 4) a second peripheral contact opening within insulative material over a second node in the peripheral circuitry area;

forming sacrificial plugging material within the bit node contact opening, the capacitor node contact opening, the first peripheral contact opening and the second peripheral contact opening;

removing sacrificial plugging material from the bit node contact opening, the first peripheral contact opening and the second peripheral contact opening while leaving sacrificial plugging material within the capacitor node contact opening; and commonly replacing the removed sacrificial plugging material with conductive material that is in electrical connection with the bit node, the first node and the second node;

after the replacing, forming the conductive material into a bit line in electrical connection with the bit node and into a local interconnect line in the peripheral circuitry area electrically interconnecting the first and second nodes; and

after forming the bit line and the local interconnect line, removing sacrificial plugging material from the capacitor node contact opening.

36. (Original): The method of claim 35 wherein prior to the removing, depositing an insulating layer and etching respective removal openings through it to the sacrificial plugging material within the bit node contact opening, the first peripheral contact opening and the second peripheral contact opening; the removing comprising etching the sacrificial plugging material from the bit node contact opening, the first peripheral contact opening and the second peripheral contact opening through the removal openings.

37. (Original): The method of claim 35 comprising after removing the sacrificial plugging material from the capacitor node contact opening, forming a capacitor of a memory cell of the memory circuitry in electrical connection with the capacitor node.

38. (Original): The method of claim 35 wherein the sacrificial plugging material comprises insulative material.

39. (Original): The method of claim 35 wherein the sacrificial plugging material comprises conductive material.

40. (Original): The method of claim 39 wherein the sacrificial plugging material comprises conductively doped semiconductive material.

41. (Original): The method of claim 35 wherein the sacrificial plugging material comprises semiconductive material.

42. (Original): The method of claim 35 wherein the sacrificial plugging material comprises insulative material and semiconductive material.

43. (Original): The method of claim 42 wherein the insulative material comprises silicon dioxide and the semiconductive material comprises polysilicon.

44. (Original): The method of claim 35 wherein the forming sacrificial plugging material within the bit node contact opening, the first peripheral contact opening and the second peripheral contact opening comprises commonly forming sacrificial plugging material within the bit node contact opening, the first peripheral contact opening and the second peripheral contact opening.

45. (Original): The method of claim 35 wherein the forming of the conductive material into the bit line and into the local interconnect line comprises lithography and etch using at least some common lithographic and etching steps.

46. (Original): The method of claim 35 comprising prior to the removing, polishing the insulative material and the sacrificial plugging material.

47. (Previously Presented): The method of claim 1 wherein the sacrificial plugging material comprises two different materials.

48. (Previously Presented): The method of claim 47 wherein the removing comprises etching, said etching comprising two different etching steps.

49. (Previously Presented): The method of claim 48 wherein the sacrificial plugging material comprises an outer material received over an etch stop material, the removing comprising etching the outer material selectively to the etch stop material.

50. (Previously Presented): The method of claim 1 wherein forming the sacrificial plugging material comprises depositing and subsequently planarizing sacrificial plugging material.

51. (Previously Presented): The method of claim 1 wherein forming the sacrificial plugging material comprises thermally oxidizing the bit node.

52. (Previously Presented): The method of claim 1 wherein forming the sacrificial plugging material comprises plasma oxidizing the bit node.

53. (Previously Presented): The method of claim 13 wherein the sacrificial plugging material comprises two different materials.

54. (Previously Presented): The method of claim 53 wherein the removing comprises etching, said etching comprising two different etching steps.

55. (Previously Presented): The method of claim 54 wherein the sacrificial plugging material comprises an outer material received over an etch stop material, the removing comprising etching the outer material selectively to the etch stop material.

56. (Previously Presented): The method of claim 13 wherein forming the sacrificial plugging material comprises depositing and subsequently planarizing sacrificial plugging material.

57. (Previously Presented): The method of claim 13 wherein forming the sacrificial plugging material comprises thermally oxidizing the bit node and the capacitor node.

58. (Previously Presented): The method of claim 13 wherein forming the sacrificial plugging material comprises plasma oxidizing the bit node and the capacitor node.

59. (Previously Presented): The method of claim 23 wherein the sacrificial plugging material comprises two different materials.

60. (Previously Presented): The method of claim 59 wherein the removing comprises etching, said etching comprising two different etching steps.

61. (Previously Presented): The method of claim 60 wherein the sacrificial plugging material comprises an outer material received over an etch stop material, the removing comprising etching the outer material selectively to the etch stop material.

62. (Previously Presented): The method of claim 23 wherein forming the sacrificial plugging material comprises depositing and subsequently planarizing sacrificial plugging material.

63. (Previously Presented): The method of claim 23 wherein forming the sacrificial plugging material comprises thermally oxidizing the bit node, the first node, and the second node.

64. (Previously Presented): The method of claim 23 wherein forming the sacrificial plugging material comprises plasma oxidizing the bit node, the first node, and the second node.

65. (Previously Presented): The method of claim 35 wherein the sacrificial plugging material comprises two different materials.

66. (Previously Presented): The method of claim 65 wherein the removing comprises etching, said etching comprising two different etching steps.

67. (Previously Presented): The method of claim 66 wherein the sacrificial plugging material comprises an outer material received over an etch stop material, the removing comprising etching the outer material selectively to the etch stop material.

68. (Previously Presented): The method of claim 35 wherein forming the sacrificial plugging material comprises depositing and subsequently planarizing sacrificial plugging material.

69. (Previously Presented): The method of claim 35 wherein forming the sacrificial plugging material comprises thermally oxidizing the bit node, the capacitor node, the first node, and the second node.

70. (Previously Presented): The method of claim 23 wherein forming the sacrificial plugging material comprises plasma oxidizing the bit node, the capacitor node, the first node, and the second node.